

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

HARI.006USH

SERIAL NO.

08/999,498

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT

Eliyahou Harari et al.

FILED

December 29, 1997

GROUP

~~1714~~ *AV 2818*

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>at</i>	A1	3	8	9	5	3	6	0	7/15/75	Cricchi et al.	365	230.03	
	A2	3	8	9	8	6	3	2	8/5/75	Spencer, Jr.	365	184	
	A3	3	9	0	6	4	5	5	9/16/75	Houston et al.	711	108	
	A4	3	9	1	4	7	5	0	10/21/75	Hadden, Jr.	365	184	
	A5	4	0	0	5	3	8	9	1/25/77	Penzel	711	173	
	A6	4	0	4	4	3	3	9	8/23/77	Berg	365	240	
	A7	4	0	5	8	7	9	9	11/15/77	George et al.	365	14	
	A8	4	0	6	4	4	0	5	12/20/77	Cricchi et al.	326	34	
	A9	4	0	9	0	2	5	8	5/16/78	Cricchi	365	184	
	A10	4	1	1	5	8	5	0	9/19/78	Houston et al.	707	1	
<i>at</i>	A11	4	1	3	0	8	9	0	12/19/78	Adam	365	184	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>at</i>	B1	0	2	8	3	2	3	8	9/21/88	Europe	—	—	NO
	B2	5	2	8	7	3	8		1/22/77	Japan	—	—	
	B3	5	8	8	6	7	7	7	5/24/83	Japan	—	—	
	B4	5	8	2	1	5	7	9	12/15/83	Japan	—	—	NO
<i>at</i>	B5	5	8	2	1	5	7	9	12/15/83	Japan	—	—	YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>at</i>	C1	J.E. Brewer et al., "Block-Oriented Random Access MNOS Memory," National Computer Conference and Exposition, Chicago, May 6-10, 1974, AFIPS Conference Proceedings, Vol. 43, pp. 837-840
	C2	J.E. Brewer et al., "Low Cost MNOS BORAM," Proceedings of IEEE National Aerospace Electronics Conference, NAECON '77, May 17-19, 1977, pp. 624-626
	C3	J.R. Cricchi et al., "Nonvolatile Block-Oriented RAM," IEEE International Solid-State Circuits Conference, Feb. 13-15, 1974, Digest of Technical Papers, pp. 204-205
<i>at</i>	C4	Raul-Adrian Cernea et al., "A 1Mb Flash EEPROM," 1989 IEEE International Solid-State Circuits Conference, pp.

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*at**09/14/98*

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JC587 04/98 86/898 PTO	FORM 1449 (8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI.006USH	SERIAL NO. 08/999,498
	INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Eliyahou Harari et al.	
			FILED December 29, 1997	GROUP 1714 <i>AV 2818</i>

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<i>at</i>	A12	4 1 4 1 0 8 1	2/20/79	Horne et al.	365	203	
	A13	4 1 9 3 1 2 8	3/11/80	Brewer	365	228	
	A14	4 2 4 1 4 2 4	12/23/80	Dickson et al.	365	195	
	A15	4 4 1 2 3 0 9	10/25/83	Kuo	365	185.33	
	A16	4 4 2 8 0 4 7	1/24/84	Hayn et al.	395	571	
	A17	4 4 3 3 3 8 7	2/21/84	Dyer et al.	702	159	
	A18	4 4 4 9 2 0 3	5/15/84	Adlhoeh	365	104	
	A19	4 4 5 1 9 0 5	5/29/84	Moyer	365	185.02	
	A20	4 4 6 0 9 8 2	7/17/84	Gee et al.	365	185.19	
	A21	4 4 6 8 7 2 9	8/28/84	Schwartz	711	172	
<i>at</i>	A22	4 5 2 1 8 5 2	6/4/85	Guttag	711	163	

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>at</i>	B6	5 9 4 5 6 9 5	3/14/84	Japan	—	—	NO
	B7	5 9 1 6 2 6 9 5	9/13/84	Japan	—	—	
	B8	5 9 1 8 6 0 1 5	10/22/84	Japan	—	—	
	B9	6 2 1 8 8 0 9 9	8/17/87	Japan	—	—	NO
<i>at</i>	B10	6 2 2 8 3 4 9 6	12/9/87	Japan	—	—	YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>at</i>	C5	Kenneth L. Short, "Microprocessors and Programmed Logic," second edition. "Ch. 13.2.2 Electrically Erasable Programmable Read Only Memory, EEPROM" Prentice Hall International, 1987, pp. 492-495
	C6	Michael D. Fitzpatrick et al., "MNOS/SOS Memory Using High-Voltage Depletion-Mode CMOS Logic," pp. 196-199, Westinghouse Electric Corp., Baltimore, MD
	C7	J.R. Cricchi et al., "The Drain-Source Protected MNOS Memory Device and Memory Endurance," <u>IEDM Technical Digest</u> , 1973, pp. 126-129
<i>at</i>	C8	Virgil Kynett et al., "An In-System Reprogrammable 32Kx8 CMOS Flash Memory," <u>IEEE J. Solid-State Circuits</u> , Vol. 23, No. 5, October, 1988, pp. 1157-1163

EXAMINER 	DATE CONSIDERED 09/17/98
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JCH 8-83) 23/98 U.S. PTO	01449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI.006USH	SERIAL NO. 08/999,498
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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>at</i>	A23	4 5 2 1 8 5 3	6/4/85	Gutttag	711	163	
	A24	4 5 2 7 2 5 7	7/2/85	Cricchi	365	184	
	A25	4 6 4 2 7 9 8	2/10/87	Rao	365	185.23	
	A26	4 6 8 5 0 8 4	8/4/87	Canepa	365	230.08	
	A27	4 7 5 8 9 8 6	7/19/88	Kuo	365	186	
	A28	4 7 5 8 9 8 8	7/19/88	Kuo	365	185.09	
	A29	4 7 6 3 3 0 5	8/9/88	Kuo	365	185.22	
	A30	4 7 8 0 8 5 5	10/25/88	Iida et al.	365	185.22	
	A31	4 7 9 6 2 3 5	1/3/89	Sparks et al.	365	189.07	
	A32	4 8 0 5 1 5 1	2/14/89	Terada et al.	371	21.1	
	A33	4 8 1 1 2 9 3	3/7/89	Knothe et al.	365	195	
	A34	4 8 1 1 2 9 4	3/7/89	Kobayashi et al.	365	185.22	
	A35	4 8 2 1 2 4 0	4/11/89	Nakamura et al.	365	195	
	A36	4 8 3 9 7 0 5	6/13/89	Tigelaar et al.	365	185.16	
	A37	4 8 4 1 4 8 2	6/20/89	Kreifels et al.	365	185.22	
<i>at</i>	A38	4 8 6 0 2 2 8	8/22/89	Carroll	365	185.09	

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>at</i>	B11	6 2 2 8 3 4 9 7	12/9/87	Japan	—	—	NO
	B12	6 3 1 8 5 9 6	1/26/88	Japan	—	—	
	B13	6 3 1 0 6 9 8 9	5/12/88	Japan	—	—	
	B14	6 3 1 8 3 7 0 0	7/29/88	Japan	—	—	
<i>at</i>	B15	6 3 2 2 5 9 9 9	9/20/88	Japan	—	—	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>at</i>	C9	Denny Cormier, "Erasable/Programmable Solid-State Memories," EDN, pp. 145-154, November 14, 1985
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1449 833) 23/98 U.S. PTO	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI.006USH	SERIAL NO. 08/999,498
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<i>at</i>	A39 4 8 6 0 2 6 1	8/22/89	Kreifels et al.	365	185.18	
	A40 4 8 6 0 2 6 2	8/22/89	Chiu	365	218	
	A41 4 8 7 8 2 0 3	10/31/89	Arakawa	365	185.09	
	A42 4 8 8 2 6 4 2	11/21/89	Tayler et al.	360	78.11	
	A43 4 8 8 7 2 3 4	12/12/89	Iijima	711	173	
	A44 4 9 2 0 4 7 8	4/24/90	Furuya et al.	711	136	
	A45 4 9 3 3 9 0 6	6/12/90	Terada et al.	365	185.21	
	A46 4 9 3 9 6 9 0	7/3/90	Momodomi et al.	365	185.17	
	A47 4 9 5 3 1 2 9	8/28/90	Kobayashi et al.	365	185.25	
	A48 5 0 3 3 0 2 3	7/16/91	Hsia et al.	365	185.12	
	A49 5 0 3 6 4 6 0	7/30/91	Takahira et al.	711	103	
	A50 5 0 4 3 9 4 0	8/27/91	Harari	365	185.03	
	A51 5 0 5 3 9 9 0	10/1/91	Kreifels et al.	711	103	
	A52 5 0 8 4 8 4 3	1/28/92	Mitsuishi et al.	365	218	
	A53 5 1 6 8 4 6 5	12/1/92	Harari	257	320	
<i>at</i>	A54 5 2 6 8 8 7 0	12/7/93	Harari	365	185.09	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

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8-83)

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at	A55 4 0 9 9 0 6 9	7/4/78	Cricchi et al.	365	218	
	A56 4 9 3 1 9 9 7	6/5/90	Mitsuishi et al.	365	185.04	
	A57 4 7 5 2 8 7 1	6/21/88	Sparks et al.	365	185.11	
	A58 4 9 7 0 6 9 2	11/13/90	Ali et al.	365	230.06	
	A59 4 9 4 9 3 0 9	8/14/90	Rao	365	185.12	
	A60 5 4 1 8 7 5 2	5/23/95	Harari et al.	365	218	
	A61 5 0 9 5 3 4 4	3/10/92	Harari	257	328	
	A62 5 1 6 3 0 2 1	11/10/92	Mehrotra et al.	365	185.03	
	A63 5 1 7 2 3 3 8	12/15/92	Mehrotra et al.	365	185.03	
at	A64 5 4 3 4 8 2 5	7/18/95	Harari	365	185.24	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C10	Colin S. Bill, et al.; A TEMPERATURE- AND PROCESS- TOLERANT 64K EEPROM, <u>IEEE Journal of Solid State Circuits</u> , Vol. SC-20, No. 5, 1985, pp. 979-985
	C11	Intel Corporation, 27F256 256K (32K x 8) CMOS FLASH MEMORY, DATA SHEET, May 1988, pp. 1-21
	C12	SEEQ Technology Incorp., 48F512 512K FLASH EEPROM - PRELIMINARY DATA SHEET, October 1988, pp. 2-1 - 2-24
at	C13	Wilson, "1-Mbit flash memories seek their role in system design," <u>Computer Design</u> , (March 1, 1989) pps. 30 and 32

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1449 83) U.S. PTO 12/23/98	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI.006USH	SERIAL NO. 08/999,498
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at	A65 4 2 7 2 8 3 0	6/9/81	Moench	365	45	
	A66 4 2 8 7 5 7 0	9/1/81	Stark	365	104	
	A67 4 5 8 6 1 6 3	4/29/86	Koike	365	104	
	A68 4 6 5 3 0 2 3	3/24/87	Suzuki et al.	365	104	
	A69 4 8 4 7 8 0 8	7/11/89	Kobatake	365	104	
at	A70 5 7 1 9 8 0 8	2/17/98	Harari	365	185.33	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C14	Stark, M., "Two Bits Per Cell Rom," <u>IEEE Catalog No. 81-CH1626-1</u> , Library of Congress No. 80-85186, Order No. 341, Spring Comp Con 1981, Feb. 23-26, Twenty-Second Computer Society International Conference, San Francisco, CA, pp. 209-212
	C15	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, <u>IEEE</u> , (1988)
	C16	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," <u>IEEE Journal Of Solid-State Circuits</u> , Vol. 23, No. 1 (February, 1988), pp. 27-33
	C17	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)
	C18	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 7A, pps. 3311-3314 (December, 1981)
at	C19	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987), pp. 460-463

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<i>at</i>	A71 5 0 9 5 4 6 1	3/10/92	Miyakawa et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A72 5 2 7 0 9 7 9	12/14/93	Harari et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A73 5 2 7 0 9 8 0	12/14/93	Pathak et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A74 5 2 7 4 5 9 9	12/28/93	Ema	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A75 5 2 9 7 0 9 6	3/22/94	Terada et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A76 5 3 8 4 7 4 3	1/24/95	Rouy	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	A77 5 3 8 8 0 8 3	2/7/95	Assar et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<i>at</i>	A78 5 6 1 9 4 5 1	4/8/97	Costabello et al.			

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>at</i>	B16 0 3 9 2 8 9 5	10/17/90	European Pat. Off.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	NO
<i>at</i>	B17 4 1 1 9 3 9 4	12/19/91	Germany	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>at</i>	C20	Nakayama et al. "A 60ns 16Mb Flash EEPROM With Program and Erase Sequence Controller". <u>IEEE Journal of Solid-State Circuits</u> , Vol. 26, No. 11, Nov. 1991, New York US, pp. 1600-1605

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